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Design and Implementation of H bridge multilevel cascaded inverter for solar PV applications

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Abstract— A multi-level cascaded inverter has also been designed for connection to renewable energy supplies. Our Multi Level Inverter's primary purpose is to synthesis the required power from a different DC source. This article deals with the multi-level inverter having 31 level interfaced with both the solar panel, another of the renewable energy resources. Smaller and industrial applications have better advantage of the this topology. The usage of high-level inverters such as the 31-level resolution rises and also the harmonics that losses of both the switching are greatly reduced. In the MATLAB/Simulink environment, the suggested model validates. Its prototype testing findings show excellent performance.

Keywords- Harmonic, Harmonic components, Harmonic source, Multilevel inverter, Voltage active filter.

I. INTRODUCTION

This really is Renewable energy resources are becoming important in the age of alternative energy sources. In addition, electrical power technology have significantly improved renewable energy uses. Many uses of sustainable power will need high energy. This multilayer inverter has provided a method to raise the voltage of both the converter beyond the compound semiconductor voltage limitations. Multi-level inverters may be achieved in several ways. These neutral dotted inverters, with flying capacitors as well as the cascading inverters are the most significant topologies. Moreover, because of its fewer harmonics, better efficiency and reduced voltage stress compared to two-tier inverters, multi-level converters have been increasingly interested in power conversion in high-strom applications[1]. Different topologies were developed and extensively researched for multilevel inverters [1]– [23]. Most important are the diode clamped [NPCs] inverter [7], the condenser clamped [8] and the cascaded H-bridge inverter with independent dc sources [9]. [43] The most important of these topologies include diode clamped [4]. A waveform staircase is generated by several level inverters. Through expanding the number of output levels, overall output voltages were increased as well as the output voltage harmonic content is decreased [10]. Therefore, this high output voltage is produced by raising the level number. Nevertheless, for specific applications, harmonic components are needed under some circumstances on an output voltage wave.

There are many kinds of inverters in literature[11] which vary in structure in the inverter suggested. It is easy to raise the level number. This reduces stress voltage, and makes it possible to produce more sinusoidal output voltage waves. The harmonic elements on a voltage wave needed for the goals of the research may also be produced appropriately. To do this, a technique is described to determine the switching equations. For many particular functions such as a harmonic content the suggested inverter is modelled. An experimental research will verify the validity of the suggested technique. The inverter is ideal to get the harmonic components needed. The It is thus very efficient to utilise that as a harmonic voltage source.

This article covers the architecture and the number of output waveforms of both the 31 level Cascado multilevel inverter This resolution is becoming more and more. The harmonics and overall harmonic distortion are substantially reduced. In particular, owing to its reduced harmonics, increased efficiency and lower voltage stress than other inverter levels, multilevel inverters have been increasingly interested in power conversions to low and high-power applications. The requirement to overcome weaknesses in solid state switching devices is indeed a multi-level inverter for use in high-voltage systems. High performance Medium-voltage power supply. Medium power sources include batteries, super condensers and solar panels. In addition, the stage with greater DC connection voltage has fewer frequency of switching and therefore lows of the switching. The waveform staircase is generated by several level inverters. The output voltages have further steps and harmonic content of the output voltage, increasing the number of output levels. Overall performance of a single multilayer inverter under cascade is presented in this article. There is a distinct construction than some inverter in just this inverter. This reduces stress voltage, and makes it possible to produce more sinusoidal output voltage waves. For so many different purposes, including harmonic content, this inverter is modeled. An experimental investigation verifies the validity of both the technique. The inverter provides the ideal performance to get the harmonic parts needed. It is thus very efficient to utilize Modified Journal paper-reg that as a harmonic voltage source. For both the output level 31 were achieved, the basic simulation circuit is built, and waveforms are produced by PWM signals. With the appropriate voltage profile, the sinusoidal waveforms are generated. As being such, the hardware has been designed with greater efficiency and reduced output switching loss. The clarity is furthermore decreased and the harmonics.

II. DESIGN ASPECT OF CASCADED MULTILEVEL INVERTER

The multi-level inverter employed well here's a 31 level cascaded inverter. The switching patterns were determined by the increased waveform level. As that of the output, overall staircase shape can be derived.

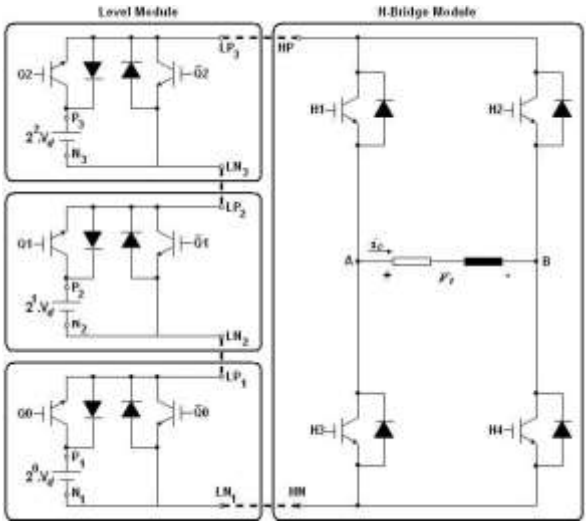

Fig.1 Configuration of the proposed single phase multilevel inverter system for 31 levels.

Table 1 shows the number of switches and output levels again for number of cascaded level modules. As shown in Table 1, a 31-level output voltage form is produced in the case of utilizing four levels of modules. That maximum value for 4 level modules remains, however, that level number. With the use of four inverter structure level modules. This pattern may be displayed in table 1. The pattern can be exhibited.

Both voltage and change for the first floor may be determined in table 1, and the following floor can be shown in table 2. Therefore, by raising the level number, the power and switch pattern are provided. They also enable several kinds of switches to improve the inverter efficiency This multilevel inverter is indeed a bridge circuit to achieve the levels that the pattern is produced in various stages. Two semi-conductive switching devices as well as a dc source is available inside the level module. This dc source voltage is shown in k=1,2,3....,m, V_d is usually represented as:

$$2^{(k+1)} * V_d \tag{1}$$

$$V_d = \frac{2.V_{\max}}{n-1} \tag{2}$$

Table.1 Voltage and Switching pattern

Voltage (p.u)	Switching pattern
15	1+2+4+8
14	1+2+8
13	1+4+8
12	4+8
11	1+2+8
10	2+8
9	1+8
8	8
7	1+2+4
6	2+4
5	1+4
4	4
3	1+2
2	2
1	1
0	0

Voltage (pu)	Switching pattern
-15	-1-2-4-8
-14	-1-2-8
-13	-1-4-8
-12	-4-8
-11	-1-2-8
-10	-2-8
-9	-1-8
-8	-8
-7	-1-2-4
-6	-2-4
-5	-1-4
-4	-4
-3	-1-2
-2	-2
-1	-1

The additional output voltage levels may be

achieved in Table 2 by raising the level number. An negative side of both the waveform gets presented. Therefore, for the 31 level output waveform, this same voltage as well as the switching pattern are provided. Depending on the number many switches utilized and produced, the number many levels may.

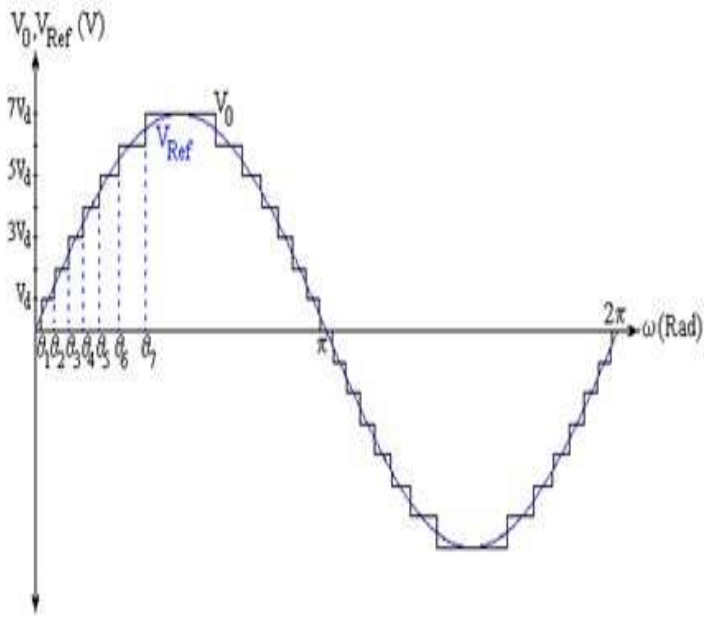

Fig.2 15-level output voltage (V_0), reference voltage wave (V_{Ref}) and switching angles (θ_1, θ_2, θ_3,. . . θ_7)

Table1 and 2 may show the increased level production. This is the number between output levels (n) and switch numbers (r).

Table.2 Number of switches and output levels related to cascaded level modules

Cascaded Level Modules	DC Source Ratio	Output Level (n) / Number of Switches (r)
LM1	$1V_d$	3
		6
LM2	$2V_d$	7
		8
LM3	$4V_d$	15
		10
LM4	$8V_d$	31
		12
:	:	:
:	:	:
LM m	$2^{(m-1)}Vd$	$2^{(m+1)} - 1$
		$2m + 4$

$$n = 2^{(m+1)} - 1 \quad (3)$$

$$r = 2m + 4 \quad (4)$$

For example, with the help of equations (5) and (6) in such a single level 31 inverter topology, the switching angles θ1, θ2, θ3, θ4, θ5, θ6 and θ7. Both output voltage and voltage waves are seen in a structure of 31 levels according the computed switching angles.

$$\theta_j = \sin^{-1}\left(\frac{2j-1}{n-1}\right) \quad (5)$$

$$j = 1,2,3,\ldots,\left(\frac{n-1}{2}\right)$$

$$V_{ref} = \frac{V_{dc}}{2} + \sum_{h=1}^{\infty} V_h \sin(h\omega t + \varphi_h)$$

$$V_{ref} = V_1 \sin \omega t + V_3 \sin 3\omega t$$

$$t_{\max} = \sin^{-1}\left(\frac{1}{2^{(m+1)} - 2}\right). \quad (2\pi f_f)^{-1}$$

$$t_{sample} = \Delta t = t_{i+1} - t_i$$

$$t_{sample} << t_{\max}$$

$$Q_0(t) = V_{ref}(t) \bmod 2$$

$$Q_0(t) = \left(\frac{V_{ref}(t) - (V_{ref}(t) \bmod 2)}{2}\right) \bmod 2$$

$$Q_{(k-1)}(t) = \left(\frac{V_{ref}(t) - (V_{ref}(t) \bmod 2^{(k-1)})}{2^{(k-1)}}\right) \bmod 2$$

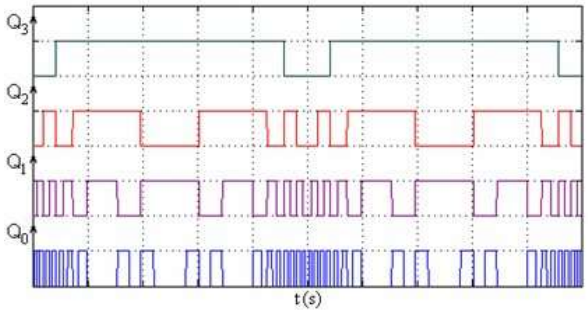

Fig.3 A sample reference output voltage wave.

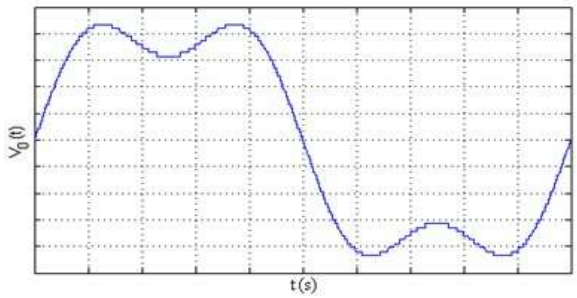

Fig.4 Switching signals in the proposed multilevel inverter including four level modules.

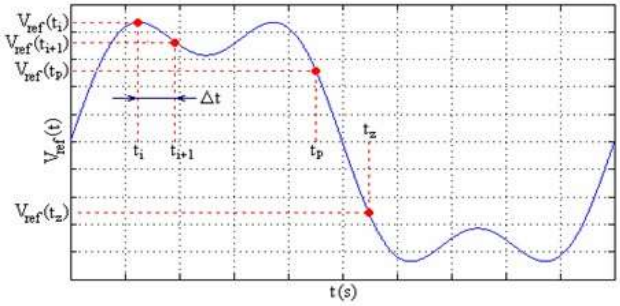

Fig.5 Output voltage of the proposed multilevel inverter including four level modules

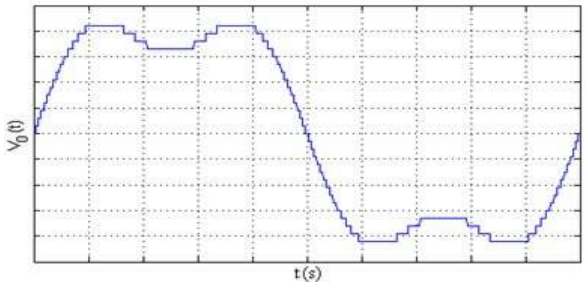

Fig.6 Output voltage of the proposed multilevel inverter including five level modules.

III. SIMULATION STUDY

This simulation model is generated using MATLAB/Simulink. For simulate actual signal control, MATLAB/Simulink is utilised. This approach may simplify a changing control system and easily convert the concept from simulation to something like a single chip execution. Fig.2 illustrates the results of the simulation of the suggested cascaded multi-level inverter. In order to evaluate other inverter levels, then simulation results regarding switching losses may also be compared. Thus, in figure 2 will be shown the output waveform. The resolution was enhanced and the results gained are plainly known. When compared with many other output power, switching losses were also reduced.

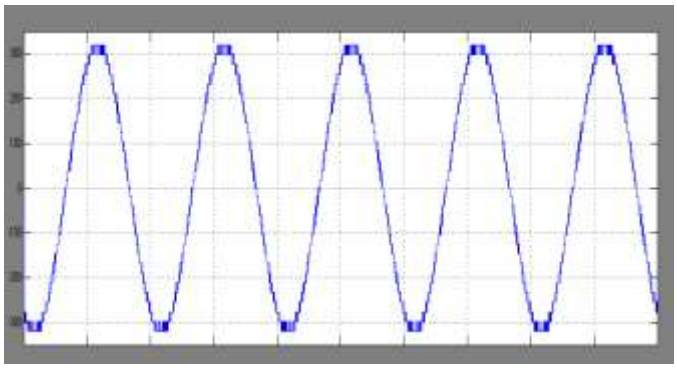

Fig.7 Output voltage waveform of 31 level cascaded multilevel inverter with resistive load

The result produced for both the simulation indicates that the resolution increases as well as the power generated by the multilayer inverter may be more than the previous levels. This is how it is described. Compared to the other levels, overall output power produced by such a 66.3W is greater. Therefore, losses are minimized by raising the levels. Figure 3 shows the waveform of the output voltage. This output voltage is determined by the supplied input. Several voltage steps are achieved throughout the output until the level output is reached. The other level has less volts.

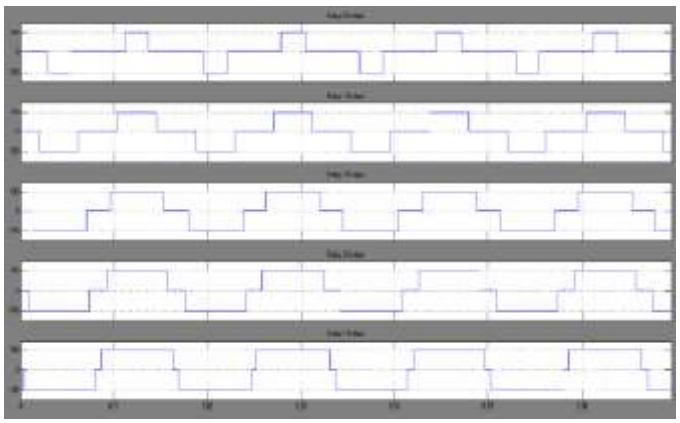

Fig.8 Output voltage waveform

By expanding the number of output levels, your output voltages may take more steps. In this situation, the output voltage type converges further to the sinusoidal waveform, which significantly reduces the THD value for a particular voltage. Simulations and tests demonstrate that now the high quality output voltage waveform is generated from this inverter architecture. Usually THD voltage values drop including for resistive loads by raising the level number. Switching strategies are simple as well as the formulation is easy to achieve using the switching angles. Increasing rise in the number with output levels for both the suggested

multi-level inverter system is simple. In this architecture pressures on power switching devices were minimized by raising the voltage number and generating a multilayer voltage wave.

IV. EXPERIMENTAL STUDY

Experimental testing of the 31-cascade multi-level inverter. A MOSFET (irf460) inverter was used to build the prototype. Throughout the configuration the voltage controls are utilized. Solar panel input DC source is provided. By the producing signal, any switching pattern is provided. This frequency of sampling was initially set at around 2 kHz as well as the frequency of output were set to 50 Hz. This dc voltage source 12 V PWM regulated in the original inverter module provides the measured output voltage as well as its corresponding voltage to examine the fundamental functioning of the 31 level inverter. It has been shown that the output power has a better resolution with efficiency increased to 97.85% with 2% of something like the losses and 7% of the total losses.

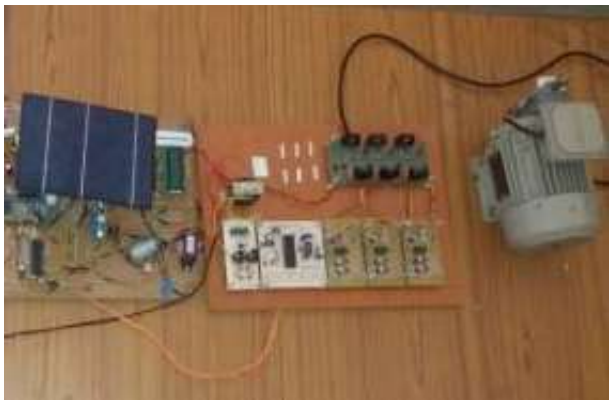

Fig.9 Experimental setup

This solar panel was utilized to transform dc into ac of both the cascaded Multilevel Inverter with input voltage inserts. As so, the output power on the dc side as well as the ac side having lower losses is increased by efficiency. The values are acquired by experiment and the results were obtained, with different loads to get the output. The resulting results are obtained. This same experiment is set up and the output for with this multilayer inverter is checked appropriately.

V. CONCLUSIONS

It has been designed to interface the 31st level cascaded multifaceted inverter for renewable energy sources. The architecture may also decrease the number of power switches needed compared to a conventional multi-level cascade inverter. Simulation and test findings including efficiency assessment have been verified. The losses of switching are smaller than the other inverter levels. The system performance by using this inverter would thus be enhanced. Furthermore, this specific situation is the basis for 97.85 per cent inverter efficiency. The findings indicate that this cascaded multistage inverter architecture may be utilized as a multistage inverter to connect with one of the renewable energy resources for small power applications and high-power applications.

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