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Design of Boost Converter with PI and IP Controllers and PI Observer

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Abstract- It is well-known that DC/DC boost converters have non-minimum phase characteristics. Using predesigned cascade controller with layered reduced-order proportional-integral observers to maintain required voltage regulation performance of cascade controller for a DC/DC boost converter despite changes in reference input, load and input voltage (PIOs). Fast-inner current control uses integral-proportional control; slow-outer voltage control uses linearized model and uses integral-proportional control. Unifying theoretical study using singular perturbation theory supports anticipated approximation of enhanced PIO system to the nominal closed-loop system using cascade controller without accounting for uncertainty. Singular perturbation theory. In order to test boost converter, computer simulations using MATLAB were conducted. Bode plot analysis of a boost converter is summarised, and it is shown system more stable with proportional-integral observers under load changes, parametric uncertainties and input voltage variations (PIOs). In order to implement boost converter, hardware is required. We discovered output voltage around 2.5 times more than input voltage both cases DC 12V battery and solar panel used to power sources.

Keywords: Cascade Control, DC–DC Power Converter, PI and IP Controllers, PI Observers, Stability.

1. Introduction

Using DC-DC power converters, the voltage supplied by source may be step up or step down to match change power need in a system and maximise energy efficiency [1]. There are frequently unexpected transient states in the dc voltage created due to varying load conditions. Converters are needed to produce a highly controlled dc voltage in these applications even though system subject to different system uncertainties, load changes parametric uncertainties and changes input voltage.

Traditional step - up converters are analysed using a mathematical model in MATLAB in order to understand the operating and design elements of conventional step-up converters. The model is used to test the circuit in a variety of real-world situations. So that improved performance may be attained in converter design, better knowledge of the challenges involved is gained. When Duty cycle is D = 0.8 and cascade controllers (PI and IP) are used, the system is more stable than when simply cascade controllers are used, according to the stability study in this work.

As a result, the outputs are nearly exactly 2.5 times as large as the inputs, thanks to the use of hardware.

2. Various Control Strategies

2.1. Pulse–Width Modulation

Pulse-width modulation, also known pulse-duration modulation (PDM), modulation method entire converting message into pulse-like signal. It is used to describe digital (binary/discrete) signals. Aside from allowing the management of power sent to electrical equipment like motors, this modulation method may also be utilised for encoding data for transmission. In this work, output signal compared reference input signal in order to create necessary pulse width modulation signal.

2.2. P–I Controller and I-P Controller

Proportional-integra1 (P-I) controller widely used to control speed of dc motor drives in past. Its capacity to maintain zero steady state error in face to step change in reference for example, simplicity of its microprocessor implementation two controller's most essential features. However, (P-I) controller number of disadvantages, including undesirable speed overshoot poor response due to fast torque changes sensitivity to controller gains$K_p and K_i$.

Forward route of (P - I) controller has terms are both proportional and integral. (P – I) controllers and (P – I) integral controllers both have ability to provide zero steady - state errors for step change using controllers. To compensate for (I - P) controller's [4] feedback, a proportionate is used in [4]. (I-P) controller, unlike (P-I) controller, does not introduce a zero they both use same mathematical formulas. As consequence, changing input reference R(S) result in reduced speed overshoot (I-P) control. Interruption load may be anticipated by both (P-I) and (I-P) controllers.

2.3. Proportional Integral Observer

Certain control methods need exact system predictions to provide closed loop control. The role of the observer is crucial here. System unknown inputs disturbances and model uncertainties can be accurately assessed, it might lead to better system performance. Control performance may be improved by using observer in addition to predicting states and unknown inputs as previously stated.

System states unknown inputs estimated using Proportional–Integral-Observer. Proportional observers may be replaced with PI-Observers when uncertain system inputs present [3]. Luenberger observer often by using classical control because its ability to state estimate system. In observer two feedback loops required. Reconstructing not just system state disturbances such as unmodelled dynamics or modelling faults done by using feedback loops both proportional and integral forms (as predicted additive inputs).

Using this technique, linear time-invariant system with unknown inputs may be represented.

$$: \dot{x}(t) = Ax(t) + Bu(t) + N\,d(x,t) + Eg(x,t)$$
$$: y(t) = Cx(t) + h(t) \qquad (1)$$

The following are the parameters of an unmodeled dynamic system:

State x (t) = Rn present time.

Input u (t) vector equals Rm,

Y (t) =R r, the measurement vector

Rl is the unknown input (d).

R is measurement noise (h)

Input d is not known (x, t),

Additive model is constructed using input matrix N. Depending method, either assuming knowledge by d(x, t) dynamics or not (disturbance observer) (Proportional-Integral observer). Matrix A, B and C known values assumed to acceptable dimensions.

3. Boost Converter PI and IP Controllers, PI Observer

Due to fact, produced DC voltage is often low, it is critical to have efficient DC - DC conversion device that can withstand unexpected transient states created by a range of industrial applications, including renewable energy. Applications need converters to provide tightly regulated dc voltage despite fact that system exposed various system uncertainties including load variations, uncertain parameters change input voltage. Cascade current mode control may be implemented with two first-order systems and obtain good performance despite system uncertainty.

Cascade control separates dynamics of current and voltage controller architecture incorporates cascading current and voltage control inner, outer loops. Systematic control design example, used back stepping strategy. Authors of this study introduced Zhong and Hornik's H control cascading current–voltage control mechanism. Adaptive controller is designed by decrease output voltage ripple due to input voltage variations. Two-loop controller incorporated sliding-mode current control, proportional–integral voltage control (PI).

This presents novel cascade controller for dc/dc boost converters. In order to get desired outcomes for nominal closed-loop system, we employed IP control for outer loop and PI control for inner loop. Nonlinear character of dc/dc boost converter may prevent linearized IP–PI cascade control technique from achieving intended performance in presence of parametric uncertainty and input voltage changes. Pre-designed cascade control structures utilise nested reduced-order PIOs to assure resilient transient performance in the face of a variety of unknowns.

For three distinct circumstances, theory and simulation were used in this research. Utilising programmable dc power supply to modify reference input, load and input dc voltage for boost converter simulation.

1. The primary contribution of this study is as follows:
2. In order to keep nominal closed - loop system performing expected using pre - designed cascade controller without taking into account different uncertainties, we employ IP–PI cascade control with layered reduced-order PIOs.
3. Closed-loop converter system's theoretical performance, required approximation is confirmed without taking into consideration uncertainties. 2.
4. In order to carry out Bode plot analysis of circuit under varying reference input, load, and input voltage, we employ programmable dc power supply.
5. A solar panel and a 12V DC battery were utilised as inputs for the hardware circuit during testing.

3.1. Cascade Control for Nominal Performance

3.1.1. Boost Converter linearized model

Fig.1 shows DC/DC boost converter subject of investigation. Output voltage control issue will be addressed. Model incorporates inductor parasitic resistanceR_L and current - sensing resistor $R_S$to account for unavoidable voltage decreases. Fig.1 result of balancing model accuracy with controller design simplicity.

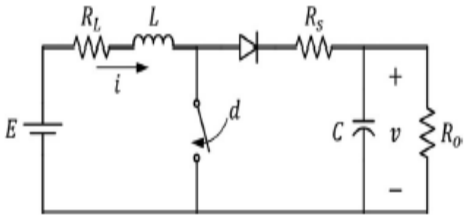


Figure 1. Boost Converter model with DC/DC $R_S and\ R_L$

Mathematical model of Fig. 1 described by

$$:\frac{\mathrm{di}}{\mathrm{d}t} = -\frac{R_L}{L}\mathrm{i} - (1-d)\left(\frac{R_s}{L}\mathrm{i} + \frac{1}{L}v\right) + \frac{E}{L} \qquad (2a)$$

$$:\frac{\mathrm{d}v}{\mathrm{d}t} = (1-d)\frac{1}{C}\mathrm{i} - \frac{1}{R_0 C} \qquad (2b)$$

E is the direct-current (DC) input, and E is the output voltage, all of which connected in series. Controlling output voltage is accomplished by varying on duration, which defined ratio of switch's on time and switching time period Ts, using Duty ratio d (0 d 1). Inductance, capacitance and load resistance are all represented by letters L, C and Ro. It assumed all factors including input voltage E unknown and/or slowly fluctuating. Equilibrium values I and d determined by when intended output voltage is $V_d(v_d > E)$.

$$: I = \frac{V_d}{(1-D)R_0} \qquad (3a)$$

$$: D = 1 - \frac{1}{2}\left[\frac{E}{V_d} - \frac{R_s}{R_0} + \sqrt{\left(\frac{E}{V_d} - \frac{R_s}{R_0}\right)^2 - \frac{4R_L}{R_0}}\right] \qquad (3b)$$

Jacobian linearization of Equation (2) equilibrium point (i, v, d) = (I v_d D) yields

$$: \dot{x}_1 = -\frac{R_1}{L}x_1 + \frac{V_1}{L}\left(u - \gamma_1 \frac{1-D}{V_1}x_2 - f_C\right) - - - -(4a)$$

$$: \dot{x}_2 = -\frac{1}{R_0 C}x_2 + \frac{1-D}{C}\left(x_1 - \gamma_2 \frac{I}{1-D}u - f_v\right) \qquad (4b)$$

It has form x = [iI] unmodelled dynamics are represented by comparable lumped disturbances, which include fc and fv as well as R1 and V1 values. Figure 2 depicts a system block diagram (4).

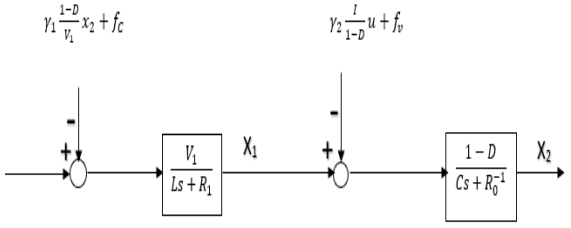


Figure 2. Linearized system block diagram

3.1.2. Cascade Control using PI & IP Controllers

Whenf_c = f_v= 0 in Fig. 2, transfer function from u to x_2 is given by

$$: G(s) = \frac{-\frac{\gamma_2 I}{C}\left(s - \frac{(1-D)V_1}{r_2 LI} + \frac{R_1}{L}\right)}{\left(s + \frac{R_1}{L}\right)\left(s + \frac{1}{R_0 C}\right) + \gamma_1 \frac{(1-D)^2}{LC}} (5)$$

For realistic circuit settings, zero is unstable [9]. Cascade two first-order minimum phase systems may be achieved in transfer function if 1 = 2 = 0. This study provides cascade controller for (5) without accounting for disturbances fc and f_v in order to achieve satisfactory nominal performance in a closed-loop converter system. A voltage-loop IP controller and a current-loop PI controller form controller's outer and inner halves, respectively. Figure 3 [4] shows two standard controllers. IP controller's closed-loop transfer function lacks extra zero, which useful for lowering output response overshoot.

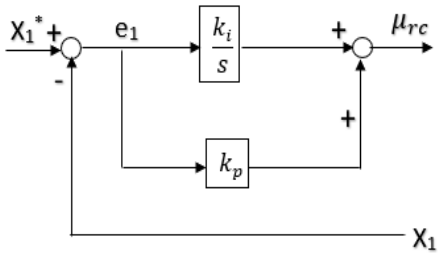
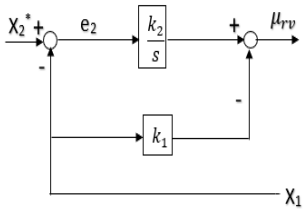


Figure 3. Controllers of Two Conventional

(A). Controller PI



(B). Controller IP

Inner-loop IP controller x1* generated by outer loop IP controller. Voltage loop's virtual control input x1* initially assumed to represent state x1 in (4b) using back-stepping technique [10]. IP controller with a feedforward cancellation term is used when x2* is intended value of x2.

$$: x_1^* = -k_1 x_2 + k_2 \int_0^t e_2 \, \mathrm{d}\tau + \frac{I}{1-D} u \qquad (6)$$

Where e2 = x2*x2 and k1 and K2 are the control gains, as shown in the figure. (b)

Closed-loop characteristics are provided by this equation.

$$: s^2 + \left(\frac{1}{R_0 C} + \frac{1-D}{C} k_1\right) s + \frac{1-D}{C} k_2 \qquad (7)$$

$$\coloneqq s^2 + 2\zeta_v \omega_v s + \omega_v^2 \qquad (8)$$

Where, ζ_v and ω_v design parameters to be determined.

Internal loop PI control adjusts duty ratio such state x1 follows reference x1*. The PI controller offers basic first-order closed-loop system, which one of many benefits of adopting it. Predictive Index controller feedforward term.

$$: u = \frac{\omega_C L}{V_1} e_1 + \frac{\omega_C R_1}{V_1} \int_0^t e_1 \, \mathrm{d}\tau + \frac{1-D}{V_1} x_2 \qquad (9)$$

E1 is defined as (x1*x1) divided by the bandwidth of the current-loop system (e1-c). The closed-loop transfer function may be proved to have the form.

$$: X_1(s) = \frac{\omega_c}{s + \omega_c} X_1^*(s) \qquad (10)$$

There's x1's Laplace transform here. Selecting a large enough bandwidth c is all that is required to get this result. If (9) and (6) are used in this situation, the control problem for (4) can be addressed.

As a result, IP–PI cascade control system was unable to meet its stated goals even though two integrators were used. This was despite fact that parametric uncertainty, input voltage variation and disturbances fc/fv all occurred simultaneously. Reduced-order PIOs nested in a closed loop make up for the performance loss of the system as a whole.

3.1.3. Robust Performance via Nested Reduced–Order PIOs

Fig. 4(a) depicts a typical first-order system with two real unknown parameters a_r , b_r, a and together with a perturbation factor f. There are two first-order systems (4 in all) involved in this method. As shown in Table 1, true properties of Figs. (4a and (4b) are listed, including a_r , b_r, a and so forth.

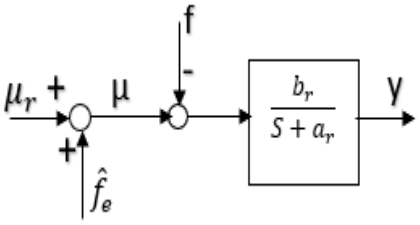
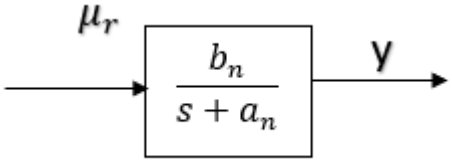


Figure 4. PIO using Performance recovery

(A). Feedforward compensation using f_e



(B). Nominal systems use of Feedforward compensation

This can be seen in Fig.5 (b) when the signal R is translated into the signals r c and r v as a reference.

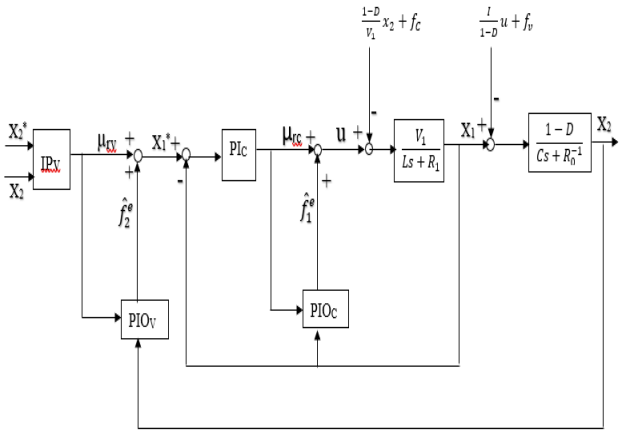


Figure 5. Nested reduced–order using PI observers Cascade Control PI & IP Controllers

Objective of reduced-order PIO in this section to design $\hat{f}_e$so that system of Fig.4 (a) behaves in same way system of Fig.4 (b) after fast transient of$\hat{f}_e$. a_n and b_n are nominal values of a_r and b_r, respectively.

System of Fig.4 (a) is described by

$$: \dot{y} = -a_r y + b_r(\mu - f) \qquad (11)$$

Where, ar>0 and br>0

Table 1. Design Converter Parameters Observer

Parameter	PIO_C (current loop)	PIO_V (voltage loop)
a_n (a_r)	R_1 / L	1 / R_0 C
b_n(b_r)	V_1 / L	(1 – D) / C
f	(1 – D) x_2 / V_1 + f_c	(I u) / (1 – D) + f_v
$\hat{f}_e$	$\hat{f}_1^e$	$\hat{f}_2^e$
μ	u	x_1^*
μ_r	μ_{rc}	μ_{rv}
y	x_1	x_2

ŚIn order account parametric uncertainties, (11) is rewritten as

$$: \dot{y} = -a_n y + b_n(\mu - f_e) \qquad (12a)$$

$$: f_e = \left(\tilde{a}y - \tilde{b}\mu + b_r f\right)/b_n \qquad (12b)$$

Where, $\tilde{a}$= a_r – a_r.and $\tilde{b}$= b_r – b_n.
When, h: = $f_e$the following system is considered model of (11):

$$: \begin{bmatrix} \dot{y} \\ f_e \end{bmatrix} = \begin{bmatrix} -a_n & -b_n \\ 0 & 0 \end{bmatrix} \begin{bmatrix} y \\ f_e \end{bmatrix} + \begin{bmatrix} b_n \\ 0 \end{bmatrix} \mu + \begin{bmatrix} 0 \\ h \end{bmatrix} \qquad (13)$$

Observer's dynamics should fluctuate slowly in order for disturbance$\hat{f}_e$. to be accurately estimated by a reduced-order observer:

$$: \dot{\hat{f}}_e = l\left(f_e - \hat{f}_e\right) = \frac{l\left(-\dot{y} - a_n y + b_n \mu - b_n \hat{f}_e\right)}{b_n} \qquad (14)$$

When observer's gain l exceeds zero, A new variable ξ is created in order to implement (14) without need for y.

$$: \xi = \hat{f}_e + \frac{l}{b_n} y$$

Or

$$\hat{f}_e = \xi - \frac{l}{b_n} y \qquad (15)$$

Using (15), reduced - order PIO is rewritten as

$$: \dot{\xi} = -l\xi + \frac{l}{b_n}(-a_n - l)y + l\mu = -l\frac{a_n}{b_n} y + l\mu_r \qquad (16)$$

With $\mu = \mu_r + \hat{f}_e$, as shown in Fig4 (a).

Singular perturbation theory and Lyapunov function technique were used in [7] to offer a robustness study of enlarged system (11) with (14). The boundedness of h is used to augment Lyapunov function technique for a unified analysis.

Substituting (11) and $\mu = \mu_r + \hat{f}_e$ into (14) yields

$$: \dot{\hat{f}}_e = \frac{l\left(a_r y - b_r\left(\mu_r + \hat{f}_e - f\right) - a_n y + b_n \mu_r\right)}{b_n} \qquad (17)$$

When observer gain l is large enough, it is possible to represent systems (11) and (17) using singular perturbation form

.

$$: \dot{y} = -a_r y + b_r\left(\mu_r + \hat{f}_e - f\right) \qquad (18a)$$

$$: \epsilon\dot{\hat{f}}_e = \frac{a_r}{b_n} y - \frac{b_r}{b_n}\left(\mu_r + \hat{f}_e - f\right) - \frac{a_n}{b_n} y + \mu_r \qquad (18b)$$

In this case, ε=1/l. There are three variables in (18) that are considered to be "slow" by singular perturbation analysis: (y), (μ_r), and (f), whereas the state $\hat{f}_e$ stable.
System (18) is stable since all parameters are positive. 18b is likewise stable and quasi-steady-state solution $\hat{f}_e$ of (18b) meets requirements for a stable system.

$$: -a_r y + \left(b_r\left(\mu_r + \hat{f}_e - f\right)\right) = -a_n y + b_n \mu_r \qquad (19)$$

Therefore, in quasi-steady-state, (18) becomes

$$: \dot{y} = -a_n y + b_n \mu_r (20)$$

Fig4's nominal system is described in this way (b). Accordingly, following a quick transient of $\hat{f}_e$in presence of parametric uncertainties and disturbance f, the nominal performance shown in Figure 4(b) may be restored by employing the reduced-order PIO technique.

Multiple integrals of estimate error may be used to simplify examination of the reduced-order PIO's performance recovery properties [11, 12].

Control input r in Fig4 (a) does not need to take into account uncertainties and disturbances in parametric parameters μ_r, as the error $\tilde{y}$ between actual and nominal systems becomes arbitrarily small 4(b)

In order to preserve required dynamic performance of nominal closed-loop system, reduced-order PIO (15), (16) is integrated with predesigned controller due to its nominal performance recovery feature. Equation $\mu = \mu_{rc} + \hat{f}_1^e$ (4a) is recast by substituting current-loop equation (4a) for current - loop equation (4a).

$$: \dot{x}_1 = -\frac{R_1}{L}x_1 + \frac{V_1}{L}\left(\mu_{rc} + \hat{f}_1^e - f_1\right) \qquad (21)$$

Where $f_1 = (1 - D)\, x_2 / V_1 + f_c$. A lumped disturbance f_1 includes (9) feedforward term.
As in (15) and (16), PIOc is designed by

$$: \hat{f}_1^e = \xi_C - l_C \frac{\bar{L}}{\bar{V}_1}x_1 \qquad (22a)$$

$$: \dot{\xi}_c = -l_c \frac{\bar{R}_1}{\bar{V}_1}x_1 + l_c\mu_{rc} \qquad (22b)$$

When lc is greater than zero. Nominal values are represented by bar symbols. Nominal system may resemble actual system (21) with (22) after a rapid transient of $\widehat{f}_1^e$.

$$: \dot{x}_1 = -\frac{\bar{R}_1}{\bar{L}}x_1 + \frac{\bar{V}_1}{\bar{L}}\mu_{rc} \qquad (23)$$

Inner-loop PI controller (PIc) is given by

$$: \mu_{rc} = \frac{\omega_c \bar{L}}{\bar{V}_1}e_1 + \frac{\omega_c \bar{R}_1}{\bar{V}_1}\int_0^t e_1\, \mathrm{d}\tau \qquad (24)$$

Where e1 = x_1^*−$x_1$and x_1^*= μ_{rv}+ $\hat{f}_2^e$ (see Fig.5). Because PIOc compensates for the feedforward term in (9) in the controller (24), term has been simplified. Closed-loop system is obtained by multiplying (24) by (23) (10). These results suggest that the goal of inner-loop control has been met by μ= μrc+$\hat{f}_1^e$.

Here's how voltage loop (4b) and closed-loop dynamics (10) are linked in cascade:

$$: \dot{x}_2 = -\frac{1}{R_0 C}x_2 + \frac{1 - D}{C}(x_1 - f_2) \qquad (25a)$$

$$\frac{1}{\omega_c}\dot{x}_1 = -x_1 + x_1^* \qquad (25b)$$

F2 = (I U) / (I D) + [fv] where at sufficiently high values of bandwidth c, the cascaded system given by equation (25) takes on a single perturbation form. Quasi-steady state solution for the boundary-layer system (25b) may be expressed asx1 =x 1*, as it is stable. Thus, $x_1^* = \mu_{rv} + \hat{f}_2^e$follows. Quasi-steady state of system (25a) is represented as

$$: \dot{x}_2 = -\frac{1}{R_0 C}x_2 + \frac{1 - D}{C}\left(u_{rv} + \hat{f}_2^e - f_2\right) \qquad (26)$$

This is PIOv for the construction of $\hat{f}_2^e$

$$: \hat{f}_2^e = \xi_v - l_v \frac{\bar{C}}{1-\bar{D}} x_2 \qquad (27a)$$

$$: \dot{\xi}_v = -l_v \frac{1}{(1-\bar{D})\bar{R}_0} x_2 + l_v \mu_{rv} \qquad (27b)$$

When lv is greater than zero. After a quick transition of $\hat{f}_2^e$, (26) with (27) may be approximated in same manner as present loop by

$$: \dot{x}_2 = -\frac{1}{\bar{R}_0 \bar{C}} x_2 + \frac{1-\bar{D}}{\bar{C}} \mu_{rv} \qquad (28)$$

Outer loop IP controller (IPv) is last stage in proposed controller architecture.

$$: \mu_{rv} = -k_1 x_2 + k_2 \int_0^t e_2 \, d\tau \qquad (29)$$

Where $e_2 = x_2^* - x_2$, and k_1 and k_2 are the control gains, respectively in this equation. This is because (28) and (29) have the same characteristic polynomial.

$$: s^2 + \left(\frac{1}{\bar{R}_0 \bar{C}} + \frac{1-\bar{D}}{\bar{C}} k_1 \right) s + \frac{1-\bar{D}}{\bar{C}} k_2 \qquad (30a)$$

$$= s^2 + 2\zeta_v \omega_v^s + \omega_v^2 \qquad (30b)$$

If k_1 and k_2 are set such polynomial (30) is Hurwitz, outer loop's control target may be met.

Without considering parametric uncertainties input voltage changes or unmodeled dynamics, PIOv and PIOc may restore the proposed IP–PI cascade controller's nominal performance with big enough lv and lc observer gains. It is recommended that $l_c > \omega_c$, and $\omega_c > l_v$ be used in the controller design. Indeed, when $\omega_v < l_v < \omega_c < l_c$, nominal system recovery is possible. It's all done by employing the equation $\mu = \mu_{rc} + \hat{f}_1^e$ to achieve control target.

4. Analysis of Stability

4.1. Analysis of Bode Plot

Bode plots used to assess stability of a system's components.
Fig. 5 illustrates Boost converter's transfer functions under various conditions:

1. Boost converter without any controllers:

$$G(s) = \frac{-4000[S-(1-D)\cdot 947\times 10^6+1270]}{(s+1270)(s+250)+(1-D)^2} \qquad (31)$$

2. Boost Converter with PI & IP controllers:

$$: G_C(s) = \frac{G(s)\cdot\left(s+\frac{k_i}{k_P}\right)k_P k_2}{(s^2+k_1k_2s)} \qquad (32)$$

3. Boost converter with PI & IP controllers along with PI observers:

$$: G_{PIO}(s) = G_C(s)\frac{(1-D)}{C(s+250)}\frac{0.378\times 10^6}{(s+1268.9)} \qquad (33)$$

4.2. Bode Plot Stability Conditions

1. Listed below are a few of the stability requirements:
2. One or both of the two margins must be positive in order for a system to be stable.
3. In a partially stable system, the phase margin should be equal to the gain margin.
4. Both of these must be positive in order to maintain stability.

4.3. Values of Analysis

Table 2 demonstrates gain margin (G.M) and phase margin (P.M) are calculated for different 'D' values.

To summarise, PI-IP controller - controlled boost converter is more stable than PI and IP controller - controlled boost converter at duty cycle D = 0.8, shown in above table 2.

4.4. Duty Ratio D = 0.8 of Bode Plots

Figures 6, 7, and 8 show Bode charts for system shown in Figure 5.

Table 2. Bode Plot Analysis Valuables

Duty Ratio (D)	Boost converter without controllers		Boost converter with PI-IP		Boost converter with PIO	
	G.M	P.M	G.M	P.M	G.M	P.M
0	0.3803	-2.4224	$1.517*10^4$	99.6208	0.013	-177.579
0.2	0.3801	-2.6841	$1.214*10^4$	102.032	5.0474	38.7958
0.4	0.38	-3.0729	$9.1178*10^3$	106.063	3.7578	31.2948
0.6	0.3807	-3.7285	$6.095*10^3$	114.144	2.4546	20.8972
0.8	0.3801	-5.2287	$3.093*10^3$	130.323	1.1119	2.534
1	0.0625	-86.4162	Inf	-74.5566	0.0123	178.898

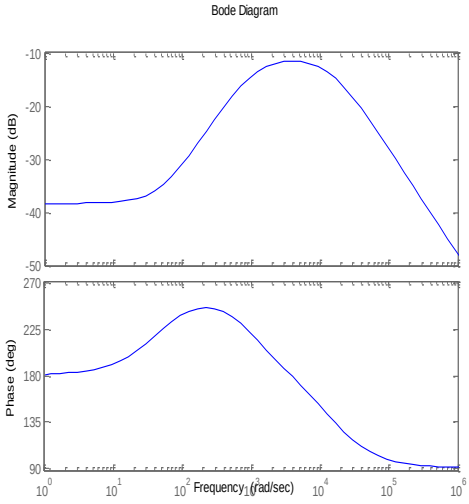


Figure 6. Boost converter Bode plot with ought controllers

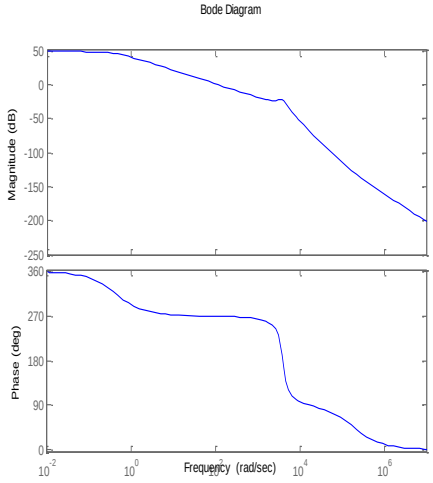


Figure 7. PI - IP controllers Boost converter Bode plot

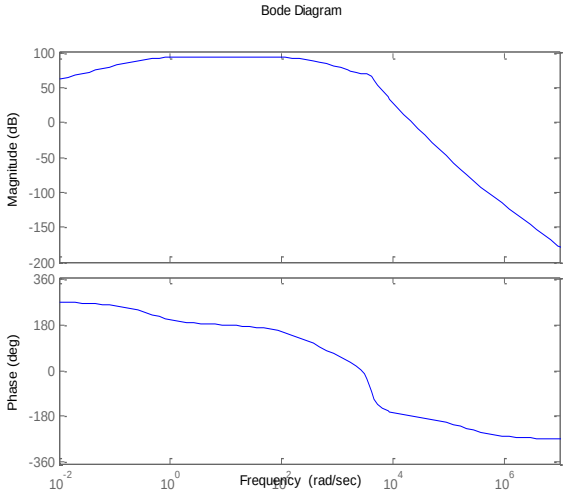


Figure 8. PI - IP controllers & PIO Boost converter Bode plot

5. Experimental result

A. MATLAB simulations were used to evaluate boost converter shown in Fig. 5 under varying loads, voltages, and reference inputs. Three different scenarios were put to the test:

B. After changing the voltage from 10 volts to 10.2 at t = 0.2 seconds, it was reverted to 10 volts again at t = 0.21 seconds, and so on.

C. An on/off switch changed load resistance from Ro =40.0 to Ro =20.0.

D. A programmable dc power supply adjusted input voltage E from 10 V to 20 V.

In computer simulations, outcomes are as follows.

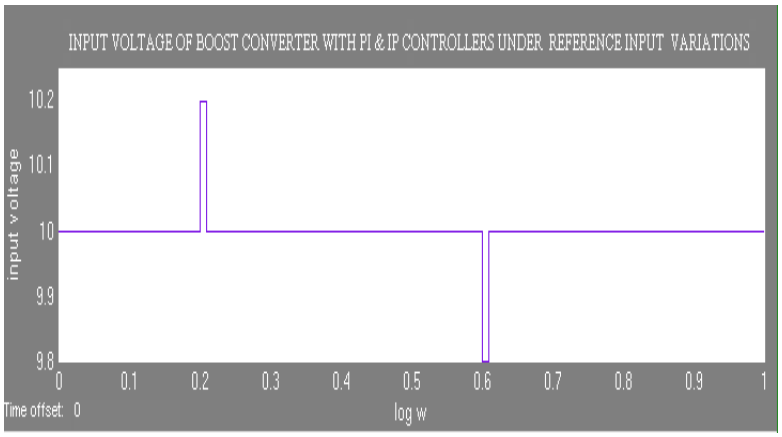


Figure 9 (A). PI - IP controllers under reference input variations of Boost converter Input voltage

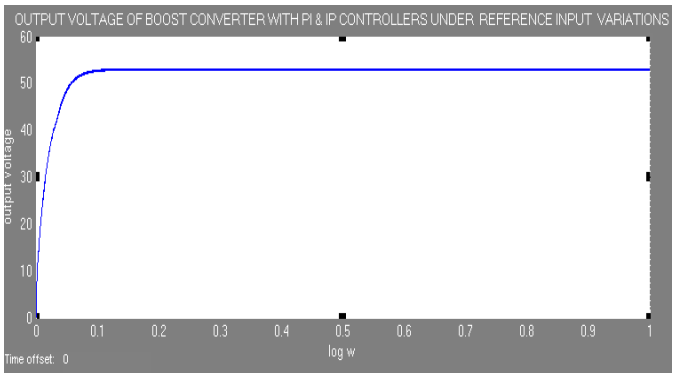


Figure 9 (b). PI - IP controllers under reference input variations of Boost converter Output voltage

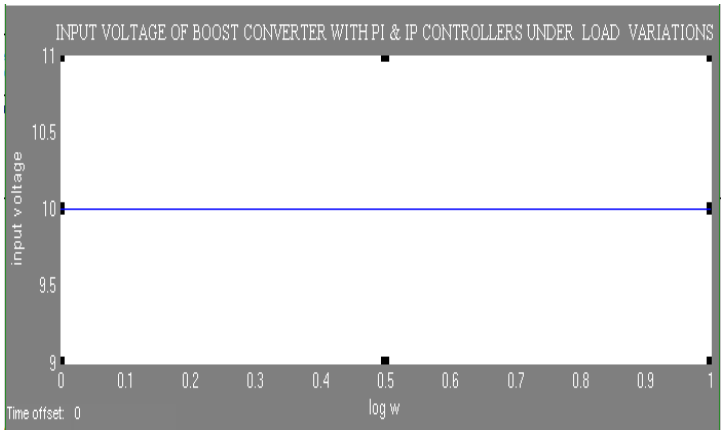


Figure 10 (a). PI & IP controllers under load variations of boost converter Input voltage

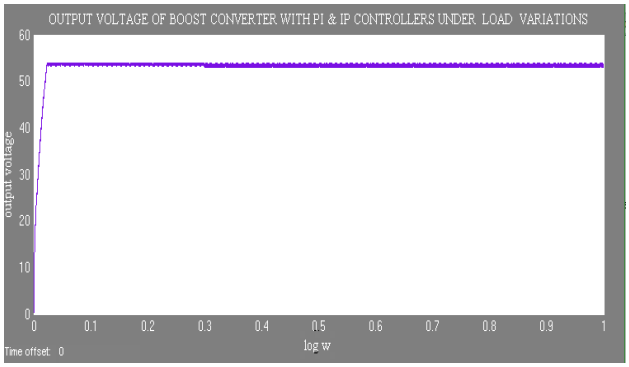


Figure 10 (b). PI & IP controllers under load variations of boost converter Output voltage

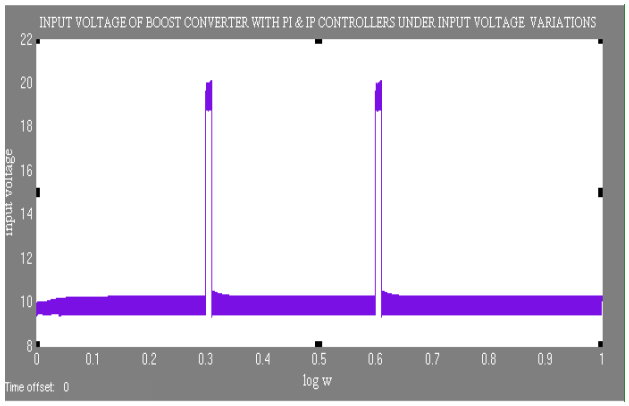


Figure 11(a). PI & IP controllers under Input voltage variations of boost converter Input voltage

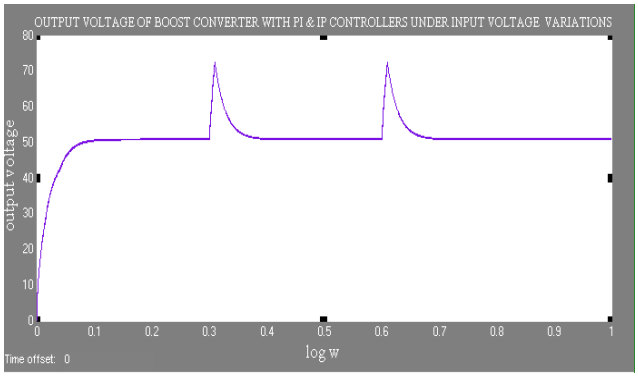


Figure 11 (b). PI & IP controllers under Input voltage variations boost converter Output voltage

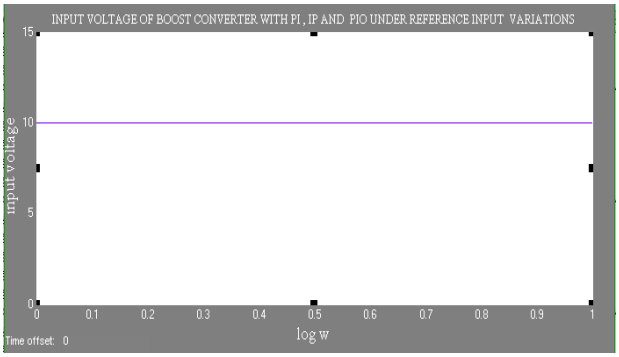


Figure 12 (a). PI & IP controllers and PIO under reference input variations boost converter Input voltage

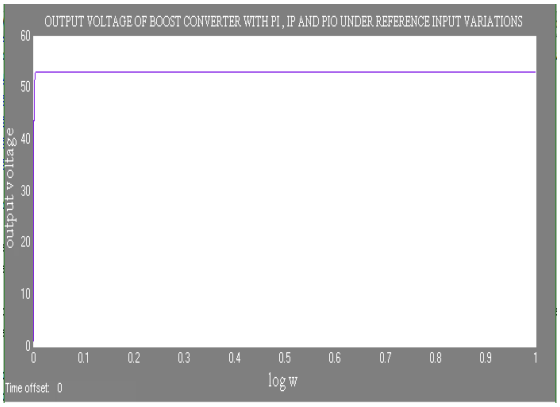


Figure 12 (b). PI & IP controllers and PIO under reference input variations of boost converter Output voltage

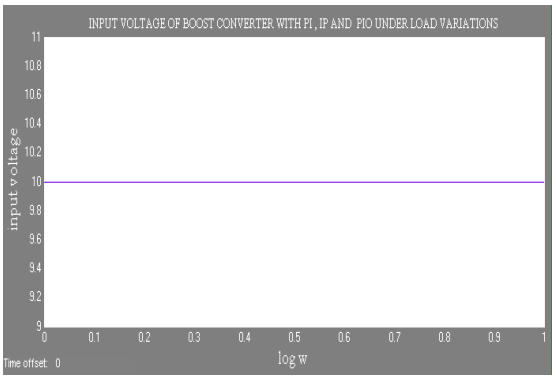


Figure 13 (A). PI & IP controllers and PIO under reference load variations of boost converter Input voltage

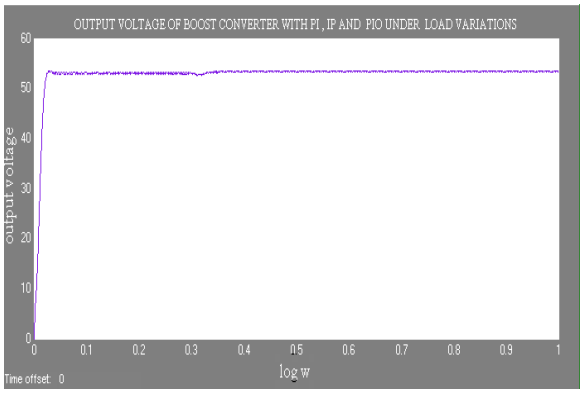


Figure 13 (B). PI & IP controllers and PIO under reference load variations of boost converter Output voltage

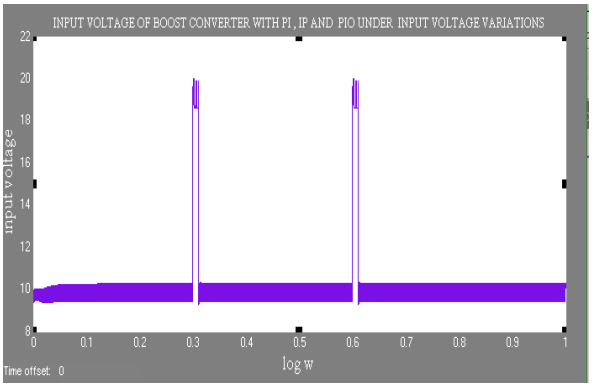


Figure 14 (A). PI & IP controllers and PIO under input voltage variations of boost converter Input voltage

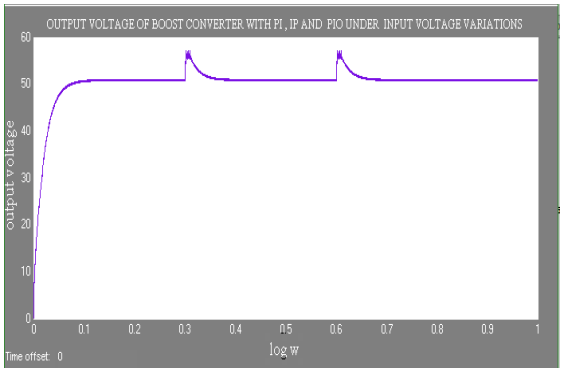


Figure 14 (B). PI & IP controllers and PIO under input voltage variations of boost converter Input voltage

Experimental findings were compared to modelled results that did not contain nested PIOs in the boost converter, as seen in the diagrams. Due to measurement noise, results are a little unsteady as results of Case A demonstrate, a system using PIOs able to retain almost nominal performance over transitional time. In cases b and c, PIO - equipped system resumed regular operation after a short transient response. According to results, proposed technique of using stacked PIOs to maintain needed dynamic performance of boost converter may be effectively implemented despite variable uncertainty in system.

6. Hardware implementation of boost converter

It was decided to build a boost converter using 555 timer, power MOSFET and potentiometer. It was decided to use 555 timer since it can reliably postpone activation of the MOSFET. Hardware implementation circuit diagram and its output when connected to DC battery of 12 V and a solar panel are presented in this work.

Power MOSFETs were employed in the boost converter shown in Figure 15 to provide the usual switch function. In order to apply the correct pulse pulses to the MOSFET, we employed 555 timers.

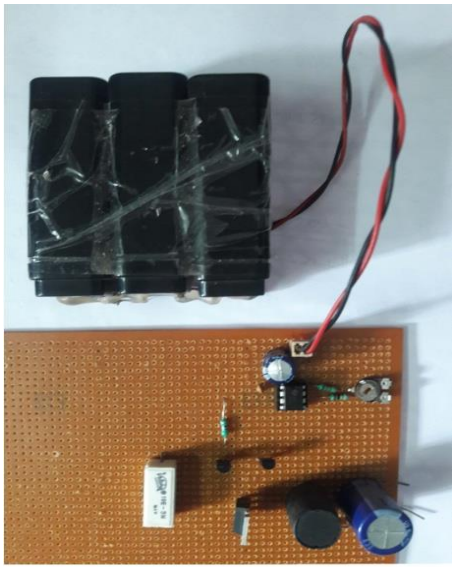


Figure 15. Boost converter Hardware implementation

In Fig. 16, the output of boost converter can be observed when linked to a DC source.

Figure 16. Boost converter DC supply Output

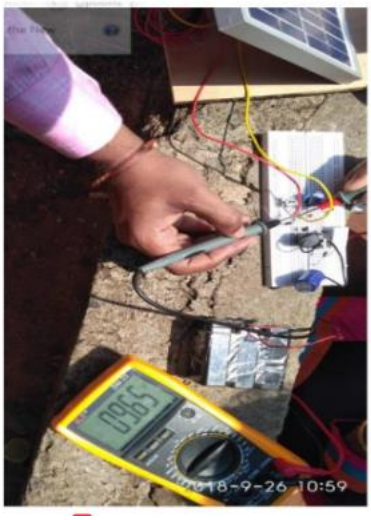


Figure 17 (A). Boost converter circuit input given by solar panel Input

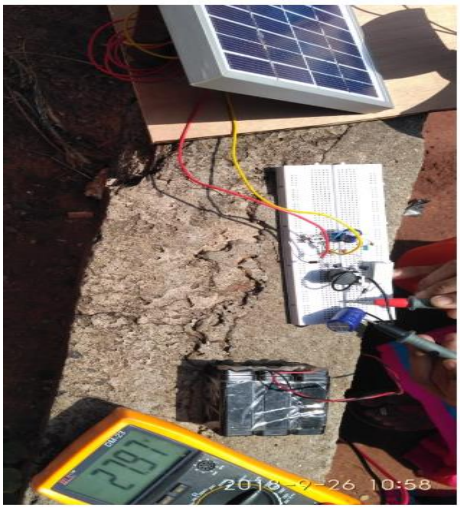


Figure 17 (B). Boost converter circuit input given by solar panel Output

Using input and output voltages, we can observe hardware - based boost converter increases voltage nearly 2.5 times.

7. Conclusion

DC/DC boost converter output voltage regulation may be improved using a new, more reliable controller, which is described in this work. Cascaded PI and IP controllers constructed for a linearized model without accounting for uncertainties in order to attain a nominally ideal dynamic response. Predesigned cascade controllers were paired with nested reduced - order PIOs to maintain intended voltage regulation performance even when faced with several unknowns during manufacturing process. Based on theory of singular perturbation and Lyapunov function, augmented closed - loop system was shown to be near to nominal closed -loop system.

Result of computer simulations, system may be utilised to manage large plant uncertainties, such as load change and parametric uncertainties.

According to bode - plot analysis, system's gain and phase margins were calculated for various duty ratios and tabulated. D = 0.8 found to be most stable setting for system.

When powered by a DC 12V battery or a solar panel, boost converter's output voltage was around 2.5 times higher than input voltage, thanks to use hardware components.

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